Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in this application.

Claim 1 (Previously Presented): In a graphics system including a main processor and a graphics processing system for generating graphics images on a display in cooperation with said main processor, and a main memory, said system including a plurality of resources requesting access to said main memory, a memory controller comprising:

a plurality of buffer memories, each of said buffer memories being operatively coupled to one of said plurality of resources requesting access to said main memory for storing information indicative of a request for main memory access;

a multiple resource buffer memory coupled to said plurality of buffer memories for storing requests for main memory access from each of said plurality of resources; and

a control circuit for controlling the transfer of information from said plurality of buffer memories to said multiple resource buffer memory, wherein said control circuit is operable to control the transfer of information from said plurality of buffer memories to said multiple resource buffer memory to reduce the frequency of switching from main memory write operations to main memory read operations.

Claim 2 (Original): A memory controller according to claim 1, wherein said plurality of buffer memories are main memory write queues.

Claim 3 (Original): A memory controller according to claim 1, wherein said multiple resource buffer memory is a main memory write queue.

Claim 4 (Original): A memory controller according to claim 1, wherein said plurality of buffer memories are main memory write queues, and wherein said multiple resource buffer memory is a main memory write queue, and wherein said control circuit is operable to control the rate at which write requests are coupled to the multiple resource buffer memory from the plurality of buffer memories.

Claim 5 (Previously Presented): A memory controller according to claim 1, wherein said plurality of buffer memories are main memory write queues and further including a plurality of main memory read queues, each read queue being operatively coupled to a resource requesting to read information from said main memory.

Claim 6 (Previously Presented): A memory controller according to claim 1, wherein said control circuit includes arbitration circuitry for arbitrating requests for access to said main memory.

Claim 7 (Previously Presented): A memory controller according to claim 6, wherein said arbitration circuitry is operable to control the frequency with which the requesting resources are enabled to participate in the arbitrating for main memory access.

Claim 8 (Previously Presented): A memory controller according to claim 1, further including a memory access control register associated with one of said resources, wherein said control circuit includes arbitration circuitry responsive to the contents of said memory access control register for determining the frequency that said resource is permitted to participate in the arbitrating for main memory access.

Claim 9 (Original): A memory controller according to claim 1, further including a set of control registers, said control registers being programmable by said main processor.

Claim 10 (Previously Presented): A memory controller according to claim 9, wherein said control circuitry is operable to arbitrate between said resources for granting requests for main memory access, wherein said control registers include a plurality of memory bandwidth control registers which are accessed by said control circuitry in determining which resource will be granted main memory access.

Claim 11 (Original): A memory controller according to claim 10, wherein each of said memory bandwidth control registers is respectively associated with a resource seeking main memory access.

Claim 12 (Previously Presented): A memory controller according to claim 9, wherein said control registers include at least one register associated with a main memory access requesting resource for storing data for said requesting resource indicative of at least one of memory usage and memory bandwidth for that resource.

Claim 13 (Previously Presented): A memory controller according to claim 9, wherein said control registers include at least one register associated with a main memory access requesting resource for storing data for said requesting resource indicative of wasted memory cycles due to granting main memory access to that resource.

Claim 14 (Original): A memory controller according to claim 1, wherein said plurality of buffer memories and said multiple resource buffer memory are write request queues, and wherein a resource that is writing to main memory generates a flush signal for initiating the flushing of that resource's write request queue.

Claim 15 (Original): A memory controller according to claim 14, further including a flush acknowledge handshake signal generating circuit that generates a flush acknowledge handshake signal to thereby indicate to competing resources that data written to main memory is actually stored in main memory rather than in an associated resource's buffer.

Claim 16 (Previously Presented): In an information processing system including a main processor, a main memory, and at least a first and a second resource competing with said main processor for access to said main memory, a memory controller comprising:

a main processor related interface including a main processor read request queue and a main processor write request queue;

a first resource related interface including at least one of a first resource read request queue and a first resource write request queue;

a second resource related interface including at least one of a second resource read request queue and a second resource write request queue;

a multiple resource write request queue for receiving requests for writing to said main memory; and

a memory access control circuit for granting access to said main memory, said memory access control circuit being coupled to receive read requests from each of said read request queues and for receiving write requests from said multiple resource write request queue.

Claim 17 (Previously Presented): A memory controller according to claim 16, wherein said memory access control circuit is operable to control the transfer of information from said main processor write request queue, said first resource write request queue and said second resource write request queue to said multiple resource write request queue to thereby reduce the frequency of switching from main memory write operations to main memory read operations.

Claim 18 (Previously Presented): A memory controller according to claim 16, wherein said memory access control circuitry is operable to arbitrate among resources competing for memory access to said main memory and to control the frequency with which requesting resources are enabled to participate in the arbitration.

Claim 19 (Previously Presented): A memory controller according to claim 16, further including a memory access control register associated with one of said resources, wherein said memory access control circuit includes arbitration circuitry responsive to the contents of said memory access control register for determining the frequency that said resource is permitted to participate in main memory access arbitration.

Claim 20 (Original): A memory controller according to claim 16, further including a set of control registers, said control registers being programmable by said main processor.

Claim 21 (Previously Presented): A memory controller according to claim 20, wherein said memory access control circuit is operable to arbitrate between said resources for granting requests for access to said main memory, wherein said control registers include a plurality of memory bandwidth control registers which are accessed by said memory access control circuit in determining which resource will be granted main memory access.

Claim 22 (Previously Presented): A memory controller according to claim 21, wherein each of said memory bandwidth control registers is respectively associated with a resource requesting main memory access.

Claim 23 (Previously Presented): A memory controller according to claim 20, wherein said control registers include at least one performance related register associated with a main memory access requesting resource for storing data for said requesting resource indicative of at least one of memory usage and memory bandwidth for that resource.

Claim 24 (Previously Presented): A memory controller according to claim 20, wherein said control registers include at least one performance related register associated with a main memory access requesting resource for storing data for said requesting resource indicative of wasted memory cycles due to granting main memory access to that resource.

Claim 25 (Original): A memory controller according to claim 16, wherein a resource that is writing to main memory generates a flush signal for initiating the flushing of that resource's write request queue.

Claim 26 (Original): A memory controller according to claim 25, further including a flush acknowledge handshake signal generating circuit to generate a flush acknowledge handshake signal and thereby indicate to competing resources that data written to main memory is actually stored in main memory rather than in an associated resource buffer.

Claim 27 (Previously Presented): In an information system including a main processor, a main memory, and at least a first and a second resource competing with said main processor for access to said main memory, a method of controlling access to said main memory comprising the steps of:

storing requests for main memory access from a first resource in a first resource request queue;

storing requests for main memory access from a second resource in a second resource request queue;

delaying forwarding requests for main memory access to a memory access control circuit to reduce the frequency of switching between memory read states and memory write states; and

granting requests for main memory access by said memory access control circuit.

Claim 28 (Original): A method according to claim 27, wherein said step of delaying includes the step of storing requests in a multiple resource write queue.

Claim 29 (Original): A method according to claim 27, further including the step of storing requests for main memory access by said main processor in a main processor request queue.

Claim 30 (Previously Presented): A method according to claim 27, wherein said step of granting requests for main memory access includes the step of arbitrating among competing resources and further including the step of controlling the frequency with which requesting resources are enabled to participate in main memory access arbitration.

Claim 31 (Previously Presented): A method according to claim 30, wherein the step of controlling the frequency includes the step of accessing contents of a memory access control register associated with a resource for determining the frequency that said resource is permitted to participate in main memory access arbitration.

Claim 32 (Previously Presented): A method according to claim 27, further including the step of controlling main memory access by programming at least one of a set of control registers in said memory controller by said main processor.

Claim 33 (Previously Presented): A method according to claim 27, wherein said step of granting main memory access includes the step of arbitrating between said resources for granting requests for main memory access, and further including the step of accessing a plurality of memory bandwidth control registers and determining which resource will be granted main memory access in part based upon the contents of said memory bandwidth control registers.

Claim 34 (Original): A method according to claim 33, further including the step of associating each of said memory bandwidth control registers with a resource seeking main memory access.

Claim 35 (Original): A method according to claim 27, further including the step of storing data relating to a requesting resource indicative of at least one of memory usage and memory bandwidth for that resource.

Claim 36 (Previously Presented): A method according to claim 27, further including the step of storing data for a requesting resource indicative of wasted memory cycles due to granting main memory access to that resource.

Claim 37 (Original): A method according to claim 27, further including the step of writing data by a resource to main memory and generating a buffer flush signal for initiating the flushing of that resource's write request queue.

Claim 38 (Original): A method according to claim 37, further including the step of generating a flush acknowledge handshake signal to competing resources that data written to main memory is actually stored in main memory rather than in an associated resource's buffer.

Claim 39 (Previously Presented): A method according to claim 27, wherein the step of granting requests includes the step of fulfilling requests for main memory access in the order requested.

Claim 40 (Previously Presented): In an information system including a main processor, a main memory, and at least a first and a second resource competing with said main processor for access to said main memory, a method of controlling access to said main memory comprising the steps of:

storing requests for writing to main memory from a first resource in a first resource write request queue;

writing to main memory by said first resource;

generating a write queue flush signal by said first resource to initiate copying information in said first resource write request queue to main memory; and

flushing said first resource write request queue.

Claim 41 (Original): A method according to claim 40, further including the step of generating a flush acknowledge handshake signal to competing resources that data written to main memory is actually stored in main memory rather than in said first resource write queue.

Claim 42 (Original): A method according to claim 40, further including the steps of

storing requests for reading from main memory from a second resource in a second resource read request queue;

comparing the main memory address associated with the read request with the addresses stored in at least one write queue; and

flushing said at least one write queue if there is a match between the main memory address associated with the read request and any of the addresses stored in said at least one write queue.

Claim 43 (Previously Presented): A method according to claim 40, further including the steps of

storing requests for writing to main memory from a second resource in a second resource write request queue;

delaying forwarding requests for memory access to a memory access control circuit to reduce the frequency of switching between main memory read states and main memory write states; and

granting requests for main memory access by said memory access control circuit.

Claim 44 (Original): A method according to claim 43, wherein said step of delaying includes the step of storing requests in a multiple resource write queue.

Claim 45 (Original): A method according to claim 40, further including the step of storing requests for main memory access by said main processor in a main processor request queue.

Claim 46 (Previously Presented): A method according to claim 40, further including the steps of arbitrating requests for main memory access among competing resources and controlling the frequency with which requesting resources are enabled to participate in main memory access arbitration.

Claim 47 (Previously Presented): A method according to claim 46, wherein the step of controlling the frequency includes the step of accessing the contents of a memory access control register associated with a resource for determining the frequency that said resource is permitted to participate in main memory access arbitration.

Claim 48 (Previously Presented): A method according to claim 40, further including the step of controlling main memory access by programming at least one of a set of control registers in said memory controller by said main processor.

Claim 49 (Previously Presented): A method according to claim 40, further including the steps of arbitrating main memory access requests between said resources by accessing a plurality of memory bandwidth control registers and determining which resource will be granted main memory access in part based upon the contents of said memory bandwidth control registers.

Claim 50 (Original): A method according to claim 49, further including the step of associating each of said memory bandwidth control registers with a resource seeking main memory access.

Claim 51 (Original): A method according to claim 40, further including the step of storing data relating to a requesting resource indicative of at least one of memory usage and memory bandwidth for that resource.

Claim 52 (Previously Presented): A method according to claim 40, further including the step of storing data for a requesting resource indicative of wasted memory cycles due to granting main memory access to that resource.

Claim 53 (Previously Presented): A method according to claim 40, further including the step of fulfilling requests for main memory access in the order requested.

Claim 54 (Previously Presented): In a graphics system including a main processor and a graphics processing system for generating graphics images on a display in cooperation with said main processor, and a main memory, said system including a plurality of resources requesting access to said main memory, a memory controller comprising:

a plurality of buffer memories, two or more of said buffer memories being operatively coupled to a different respective one of said plurality of resources requesting access to said main memory and storing information indicative of a request for main memory access from that one of said plurality of resources;

a multiple resource buffer memory coupled to said plurality of buffer memories; and

a control circuit for controlling the transfer of requests from said plurality of buffer memories to said multiple resource buffer memory, wherein said control circuit is operable to control the transfer of the requests from said plurality of buffer memories to said multiple resource buffer memory to reduce the frequency of switching from main memory write operations to main memory read operations.